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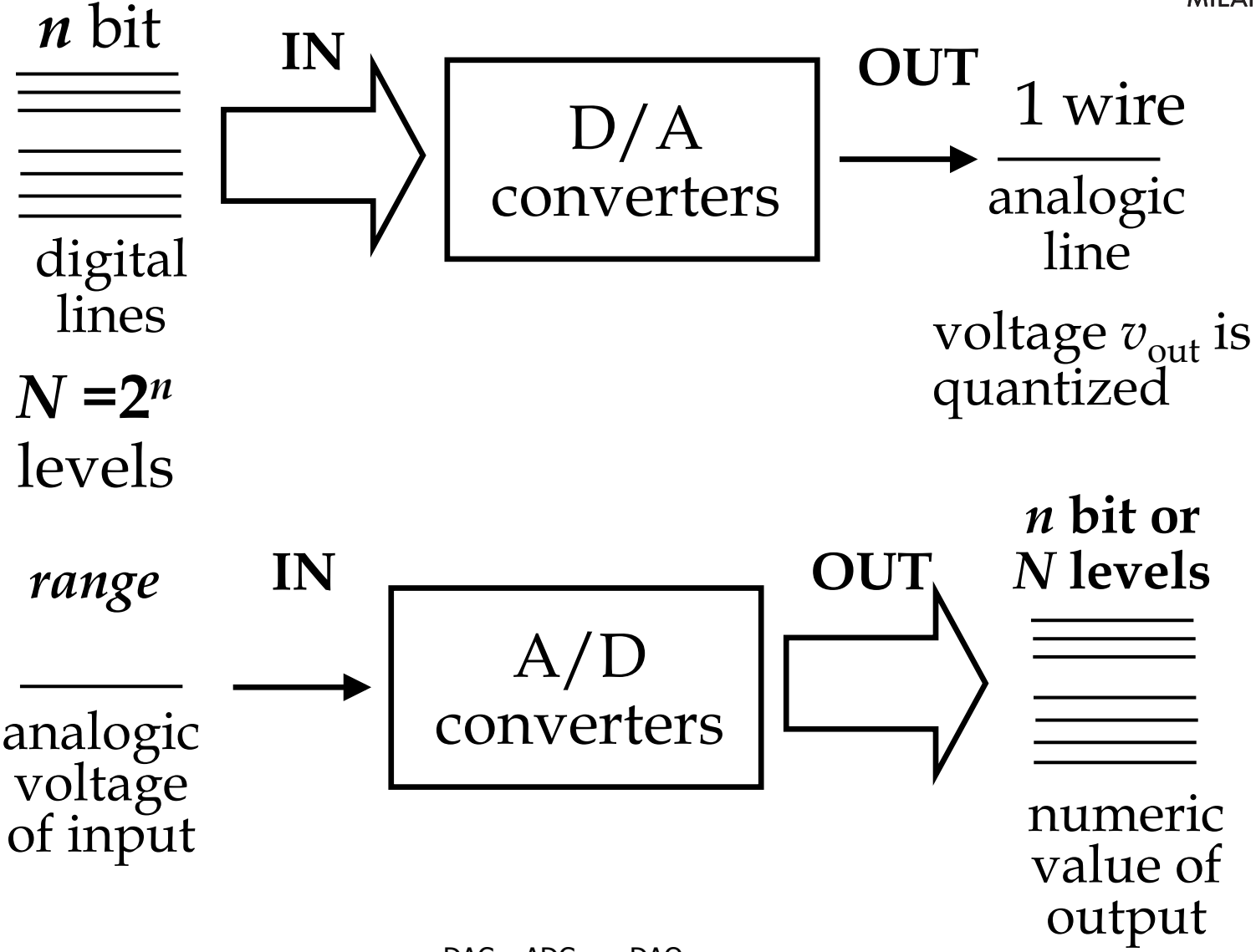
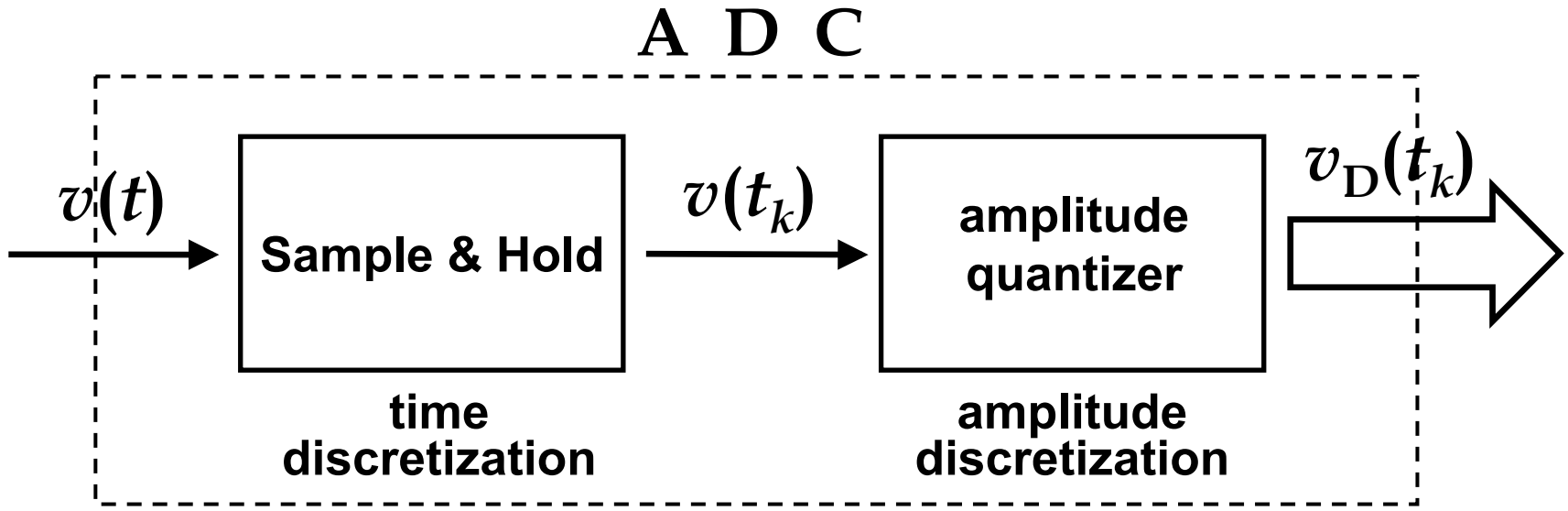
D/A E A/D CONVERTER for DAQ BOARDS

D/A e A/D Converters



Voltmeter or A/D Converter

It 's an instrument receiving as an input an analog voltage and digitizes it (first: discretizing it in time domain and then in the amplitude domain):



In particular, the quantization in the time domain takes place with a resolution $T_c=1/f_c$ (period [s] and frequency [Sa/s] of sampling)

Discretization process (1/3)

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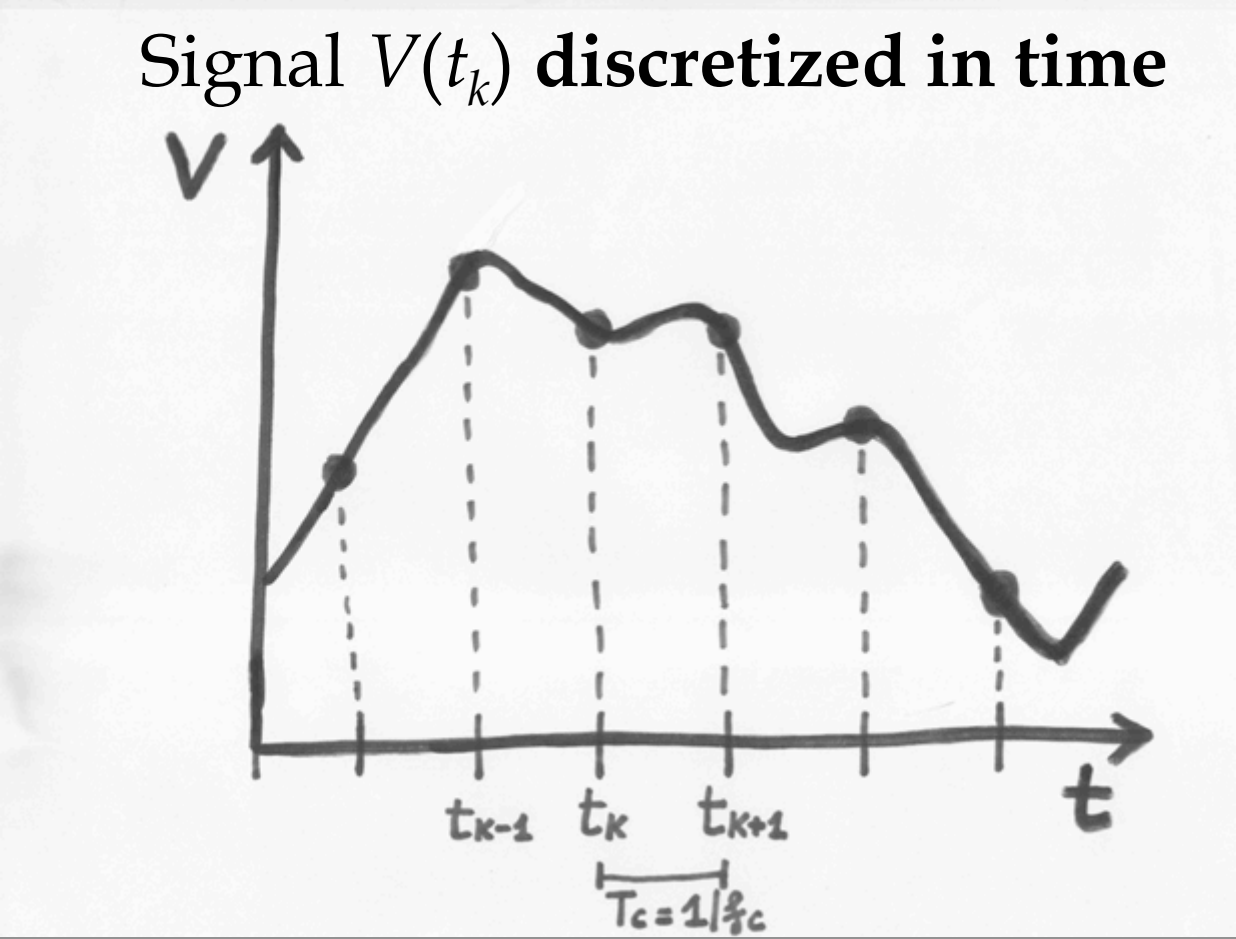
Analogic $V(t)$ signal

(the signal is **continuous** both in time and in amplitude)

Discretization process (2/3)

Signal $V(t_k)$ **discretized in time**



(the signal is still continuous or "analog" in width, but the samples are only available in discrete time)

Discretization process (3/3)

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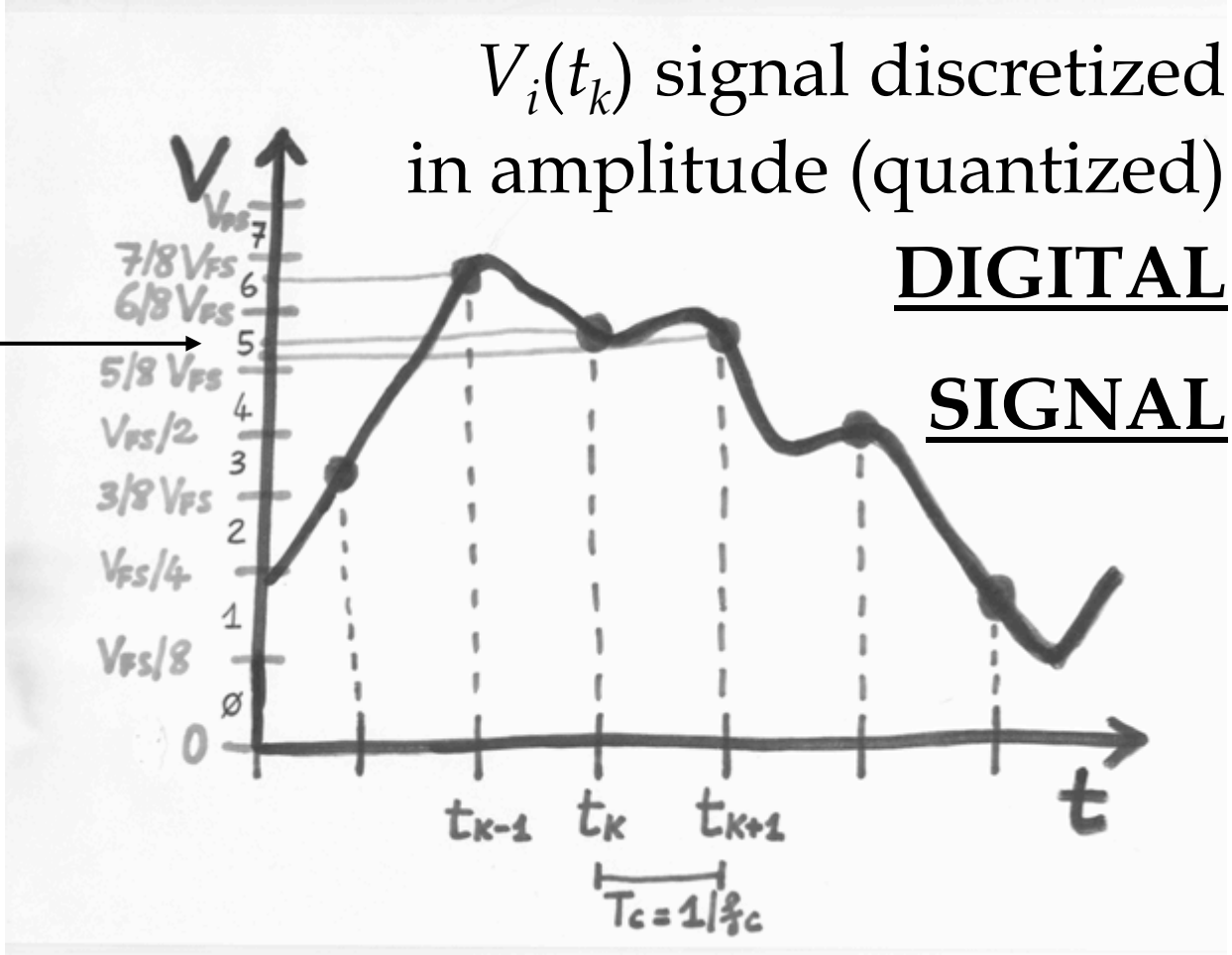
different values of analog voltage is encoded with the same numeric value. You lose information!

$V_i(t_k)$ signal discretized in amplitude (quantized)

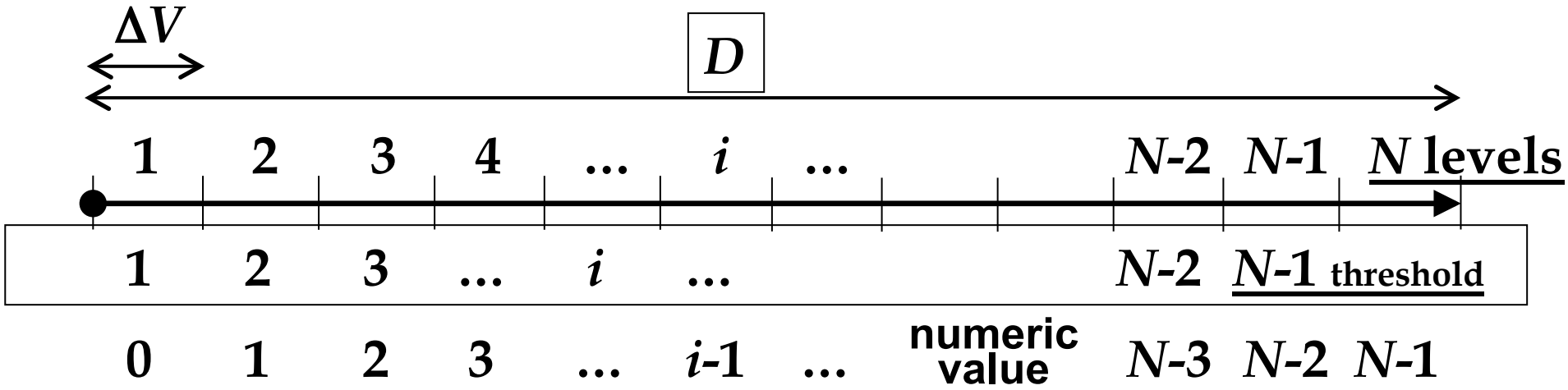
DIGITAL SIGNAL



(the digital signal is encoded into numbers)

Amplitude quantizzation

The quantization in amplitude occurs subdividing the dynamic of measure (range of values of the input analog voltage measurable) in N subintervals (levels) of constant width $\Delta V = D/N$ **(resolution)**

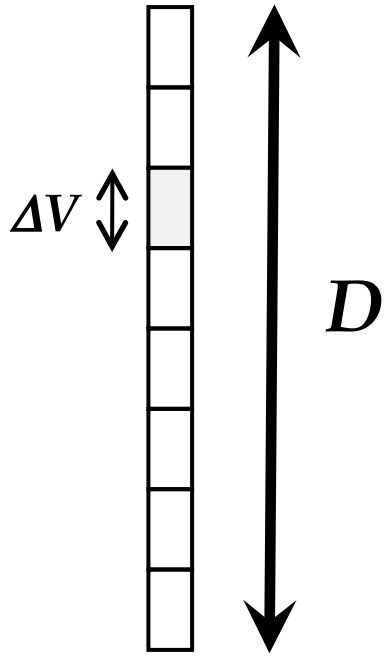


The analog voltages that fall in the range ith associates a numerical value corresponding to the i-1 integer (from 1 to N-1) that identifies the interval.

Variance and quantization uncertainty

The variance associated with the finite resolution **ΔV is**

$$\sigma_q^2 = u_q^2 = \frac{(\Delta V)^2}{12}$$

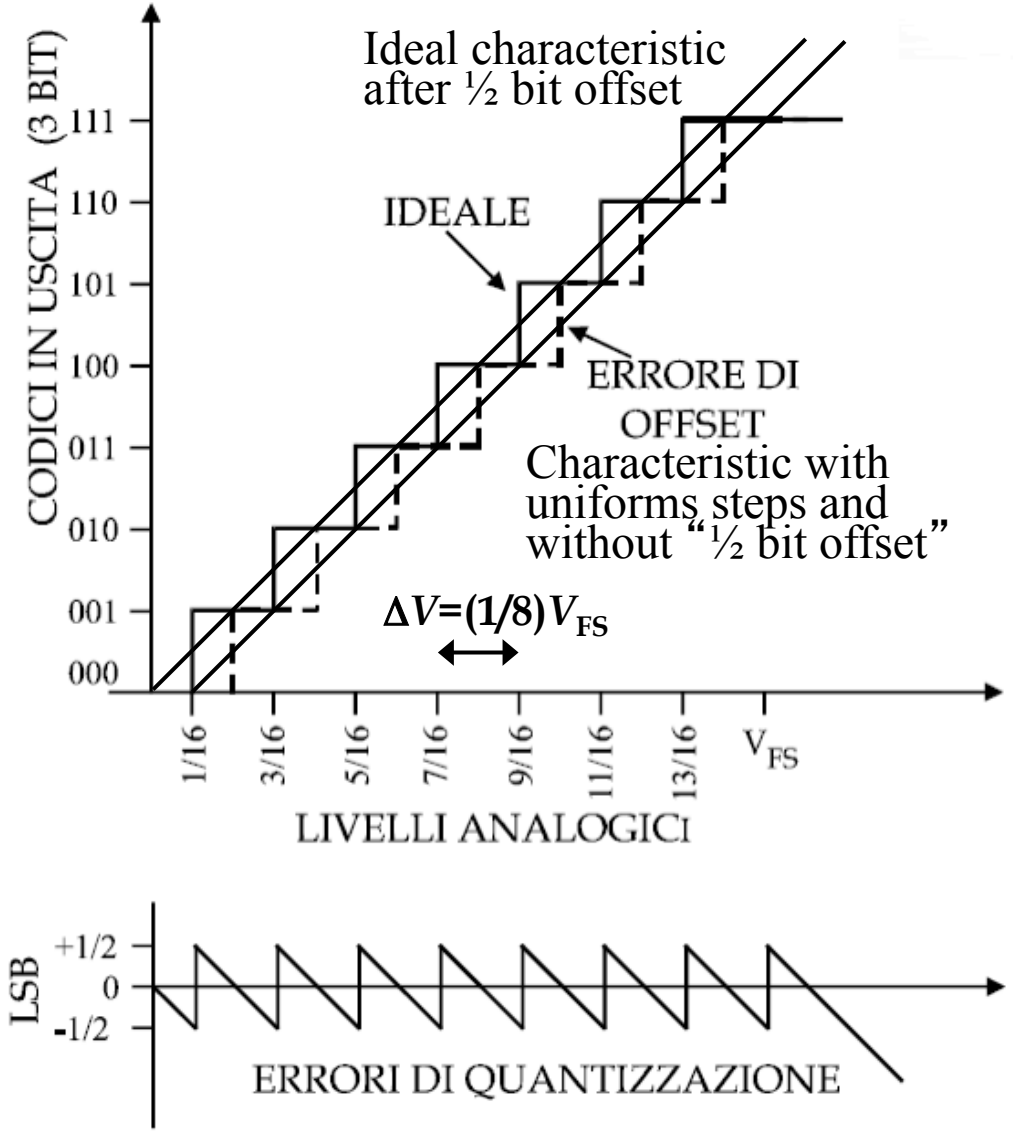


The result comes from the calculation of variance σ^2 for a PDF uniform probability range with full width ΔV

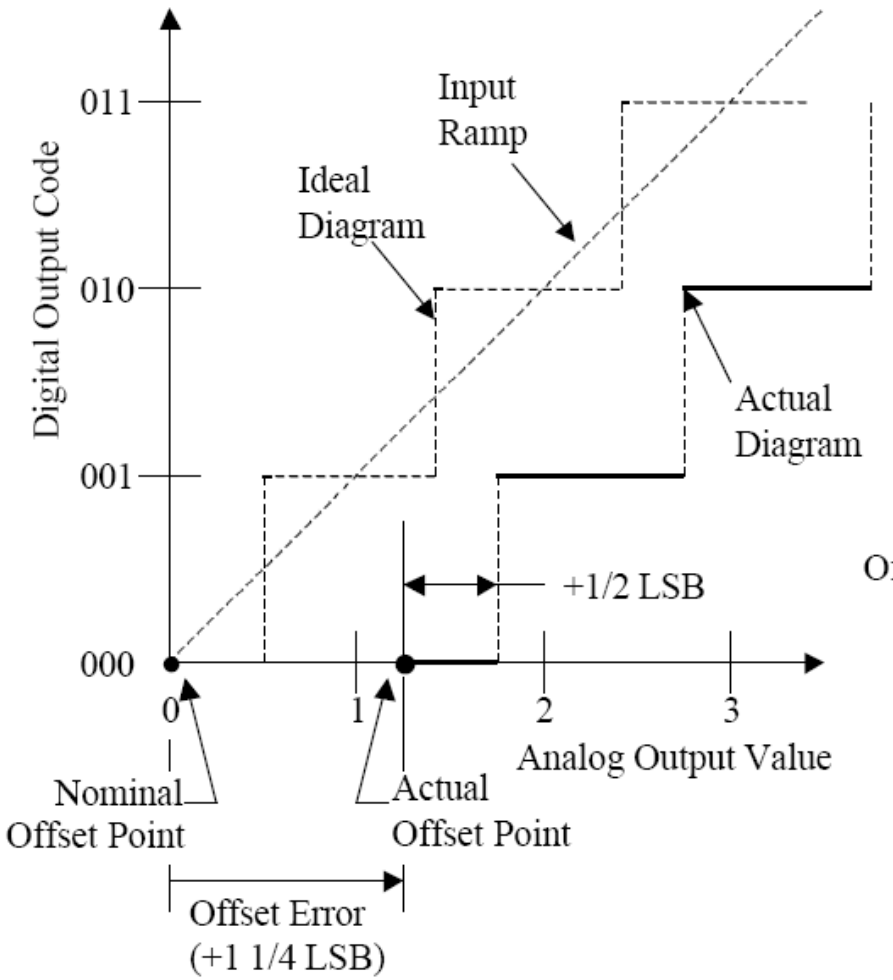
The quantization uncertainty is

$$u_q = \sigma_q = \frac{\Delta V}{\sqrt{12}}$$

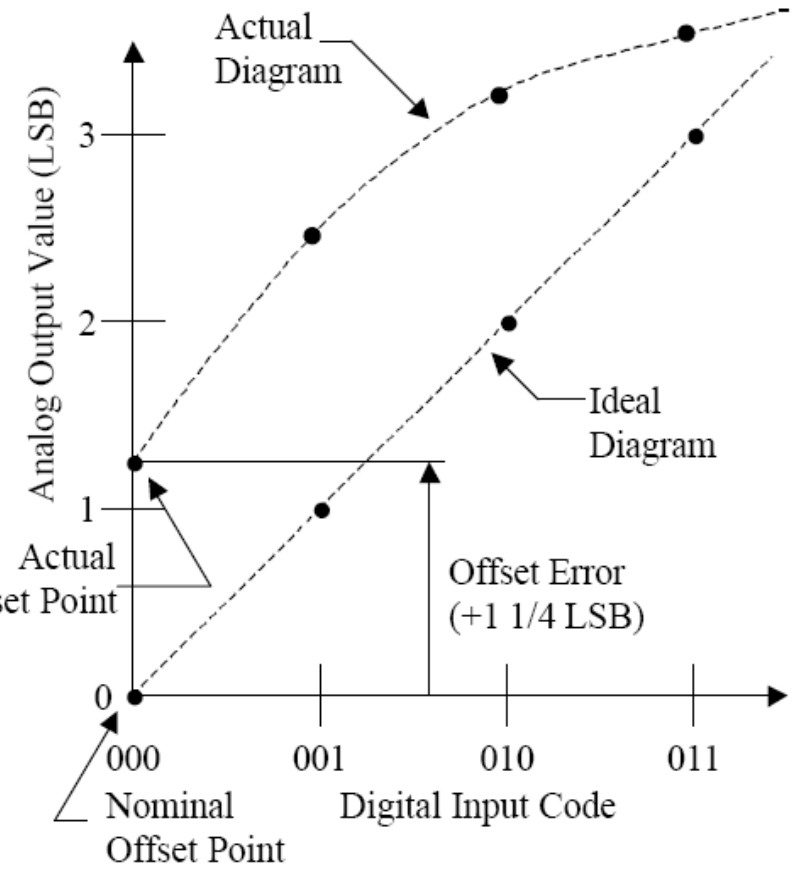
Errors in converters: quantization



Errors in conv. A/D: *offset*

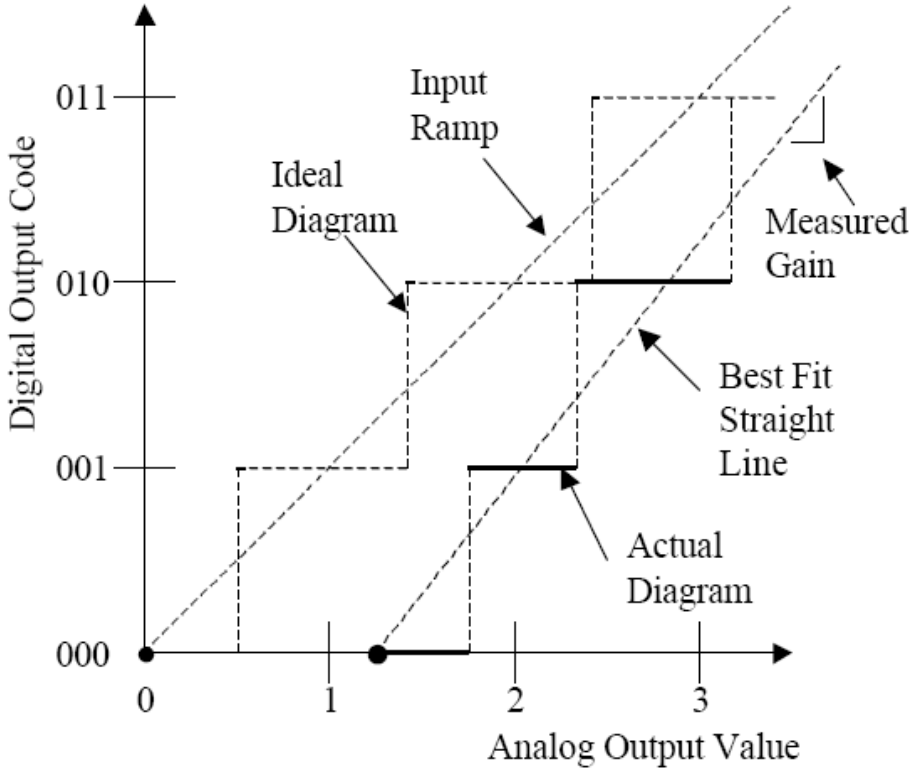


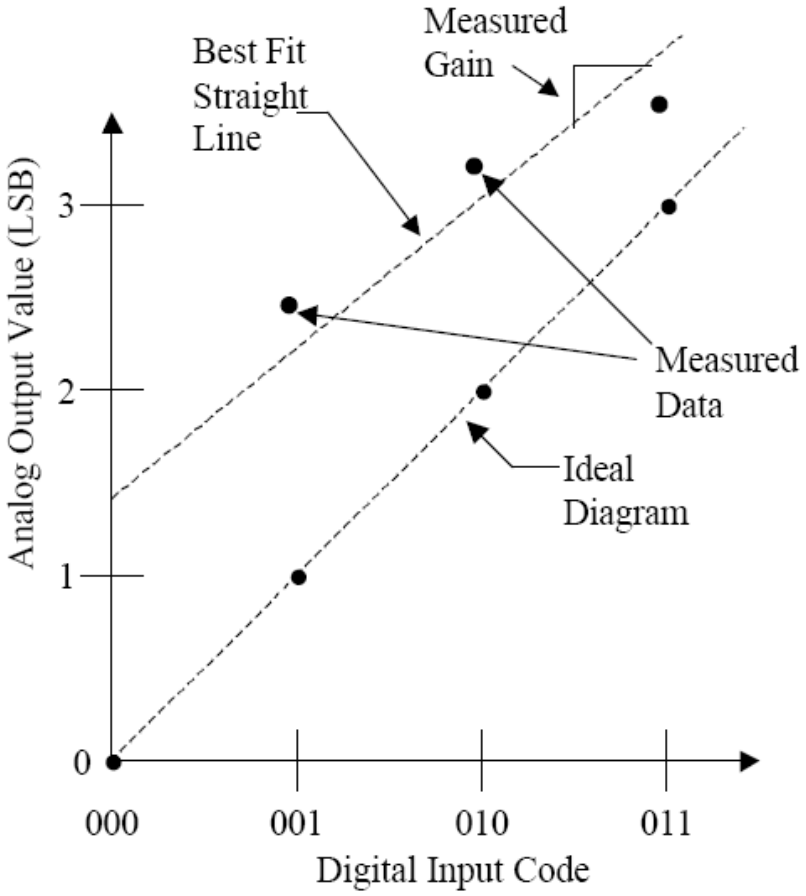
ADC



DAC

Errors in converters: *gain*

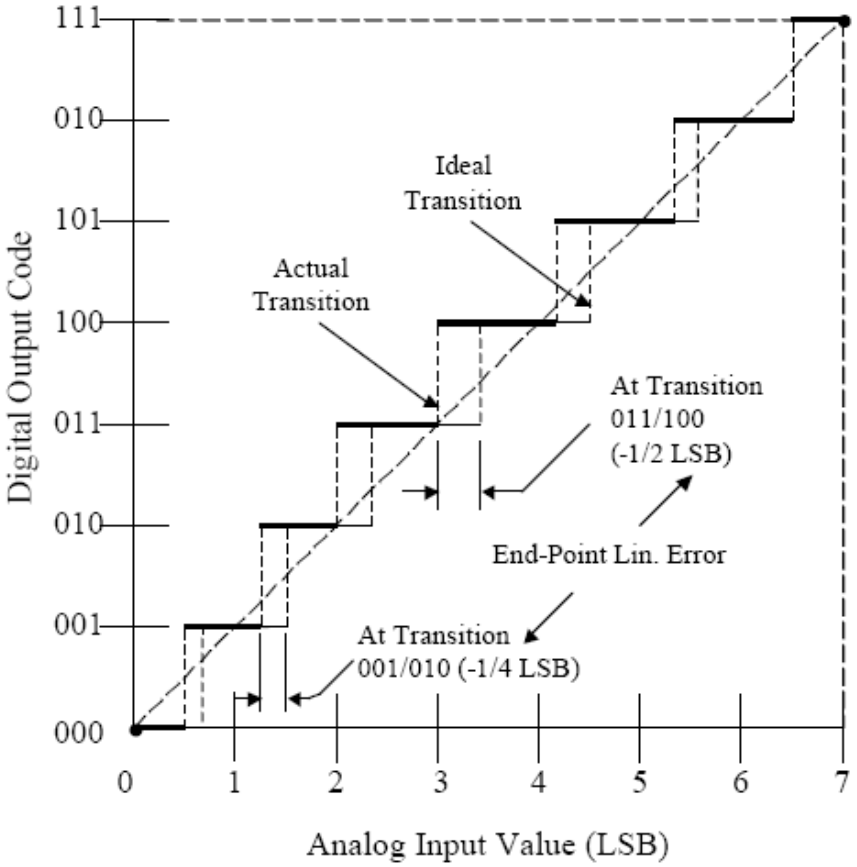




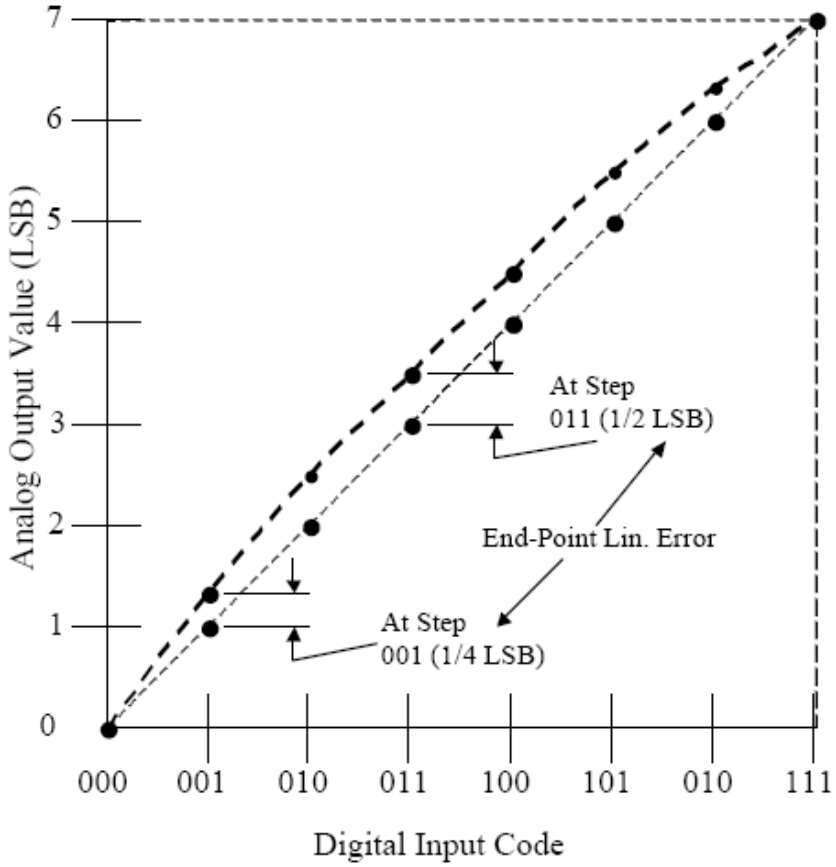
ADC **DAC**

Errors in converters: *INL*

Integral Non-Linearity error



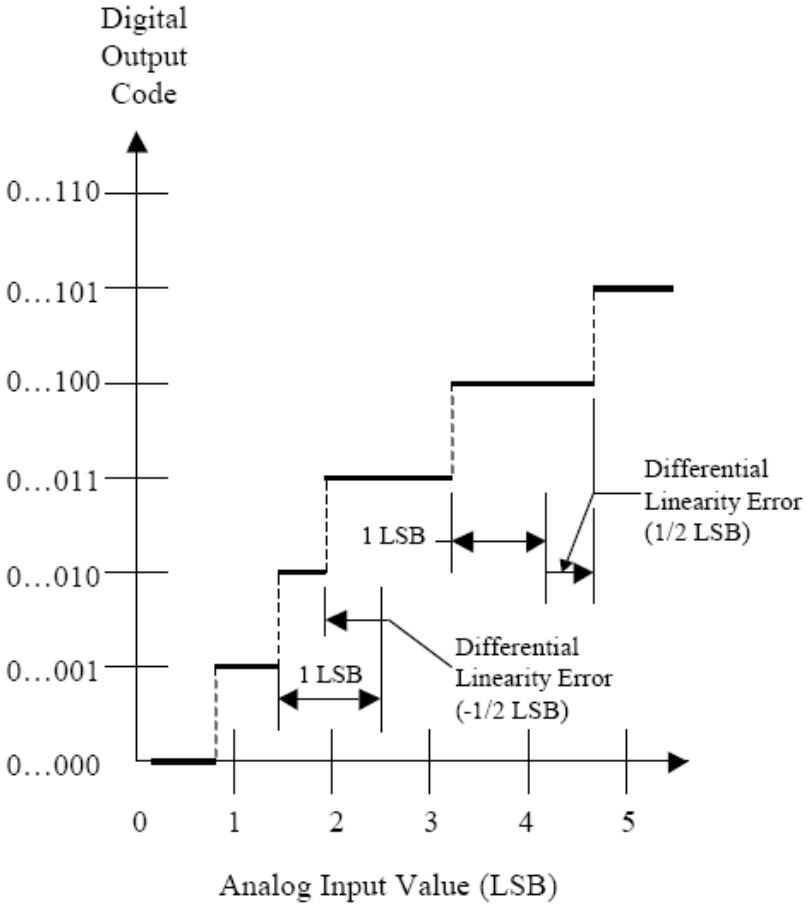
ADC



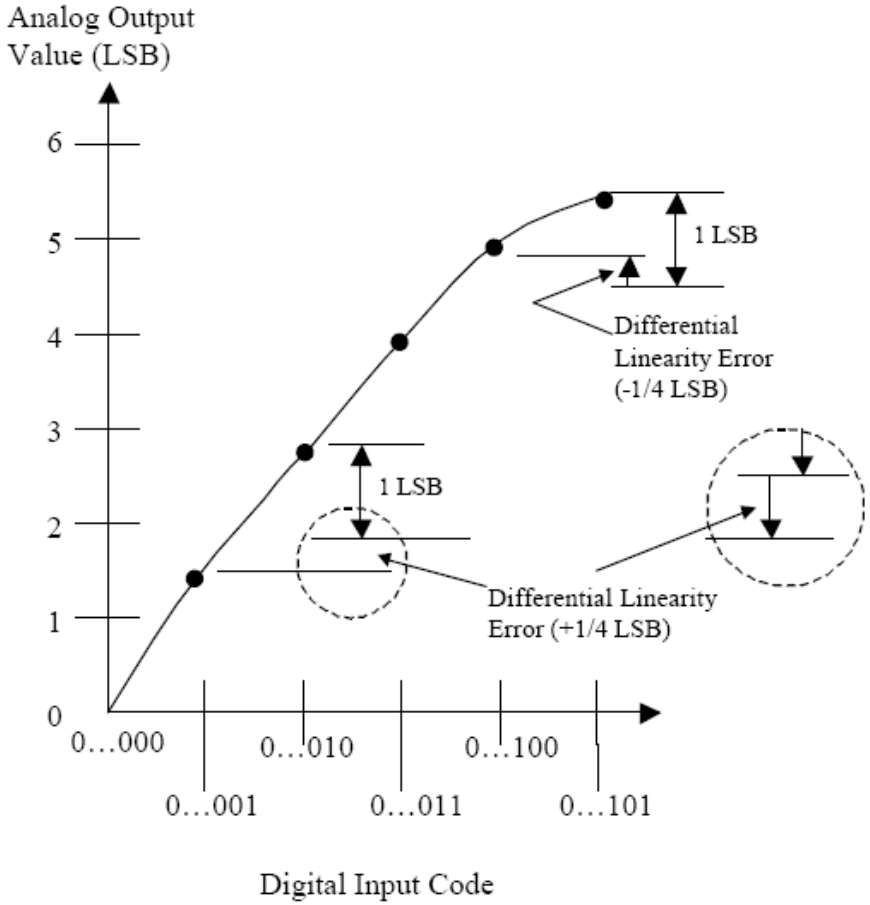
DAC

Errors in converters: *DNL*

Differential Non-Linearity error



ADC



DAC

Signal sampling (1/3)

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Shannon theorem

To be able to reconstruct a signal with limited bandwidth, you are required sampling frequency

$f_c > 2 f_{max}$ **with** f_{max} **maximum frequency (bandwidth) of the signal**

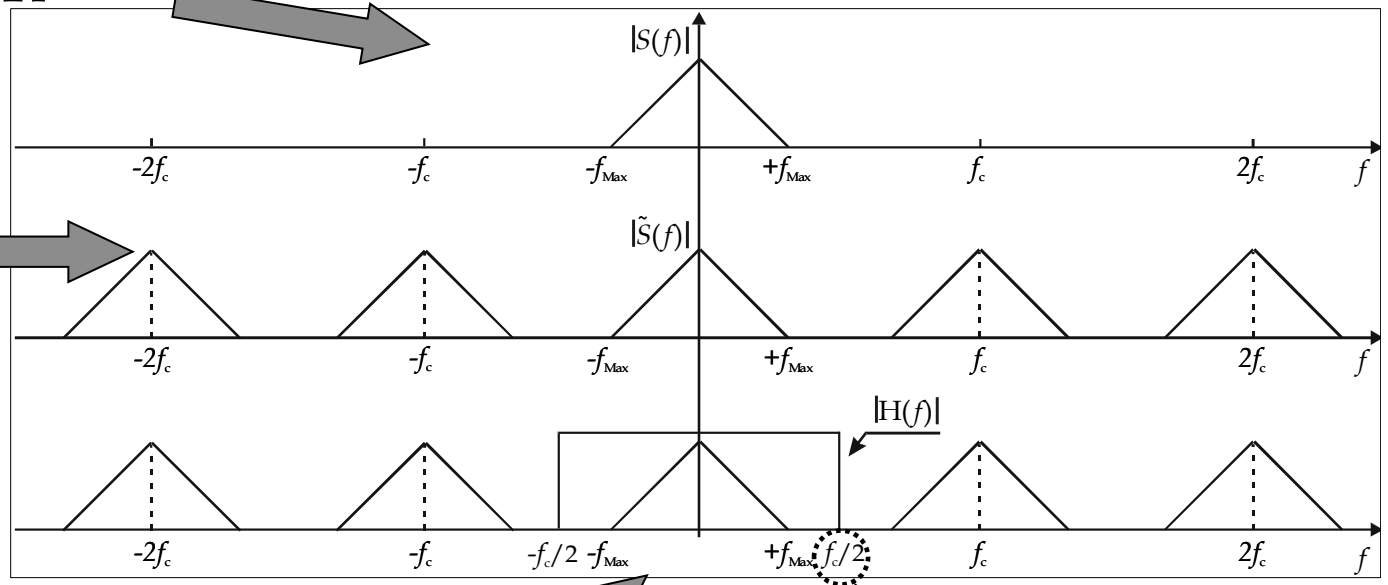
Otherwise **aliasing** phenomena occurs, which make losing important information and do not allow the correct reconstruction of the signal by low-pass filtering. In fact, the discretization in time induces a periodicity in frequency: there must be no overlaps (alias) between spectral replicas

Signal sampling (2/3)

CASE I: $f_c > 2 f_{max}$ **[correct sampling]**

Signal spectrum

Spectrum of the sampled signal



Spectrum of the sampled signal reconstructed by filtering

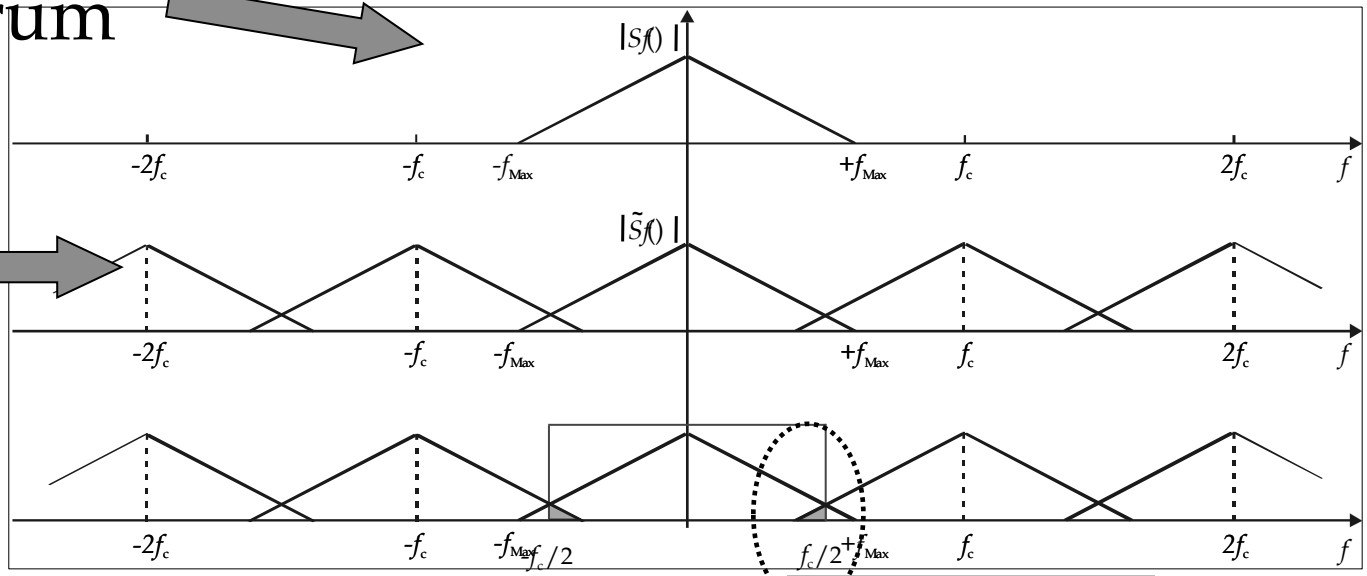
Nyquist frequency

Signal sampling (3/3)

CASE II: $f_c < 2 f_{max}$ **[downsampling]**

Signal spectrum

Spectrum of the sampled signal



aliasing

Spectrum of the sampled signal reconstructed by filtering

Effect of sampling error (*jitter* of T_c)

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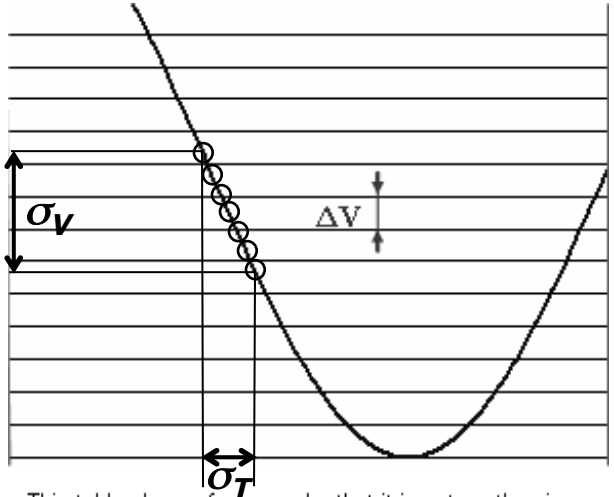
Imagine that we are digitizing a sine wave $x(t) = A\sin 2\pi f_0 t$. Provided that the actual sampling time *uncertainty* due to the *clock jitter* is Δt, the error caused by this phenomenon can be estimated as $E_{ap} \leq |x'(t)\Delta t| \leq 2A\pi f_0 \Delta t$.

One can see that the error is relatively small at low frequencies, but can become significant at high frequences.

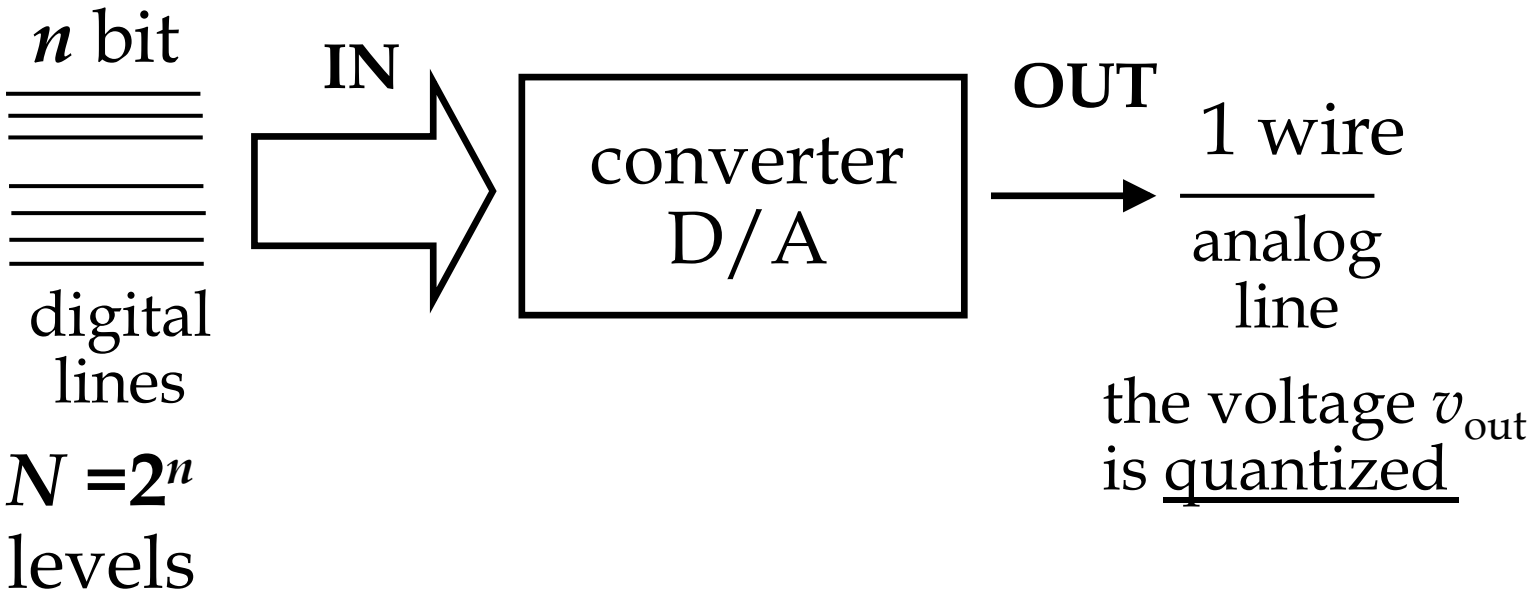
This effect can be ignored if it is relatively small as compared with *quantizing error*. Jitter requirements can be calculated using the following obvious formula: $\Delta t < \frac{1}{2^q \pi f_0}$, where q is a number of ADC bits.



ADC resolution	Input frequency				
	44.1 kHz	192 kHz	1 MHz	10 MHz	100 MHz
8	28.2 ns	6.48 ns	1.24 ns	124 ps	12.4 ps
10	7.05 ns	1.62 ns	311 ps	31.1 ps	3.11 ps
12	1.76 ns	405 ps	77.7 ps	7.77 ps	777 fs
14	441 ps	101 ps	19.4 ps	1.94 ps	194 fs
16	110 ps	25.3 ps	4.86 ps	486 fs	48.6 fs
18	27.5 ps	6.32 ps	1.21 ps	121 fs	12.1 fs
24	430 fs	98.8 fs	19.0 fs	1.9 fs	190 as

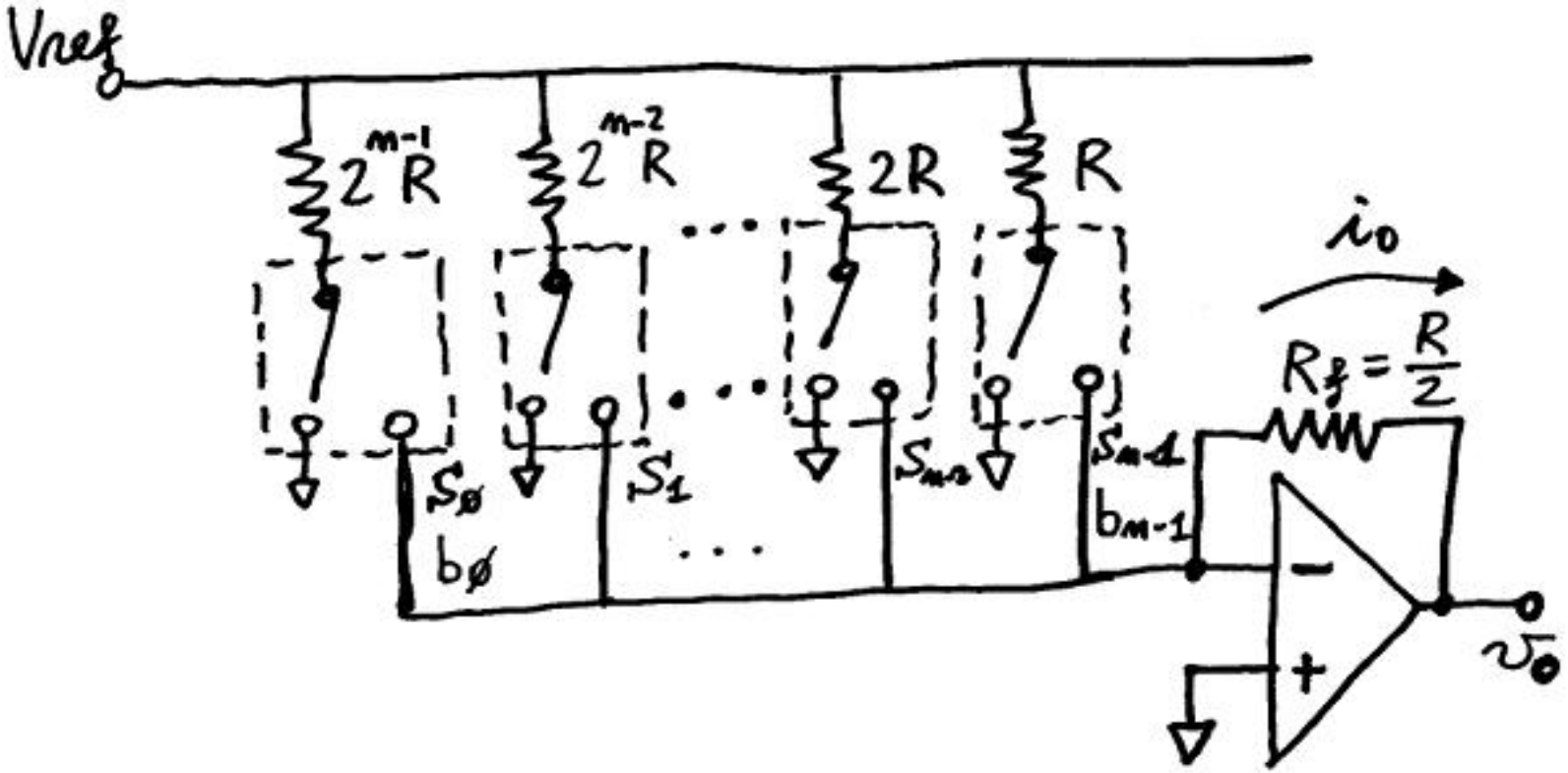
This table shows, for example, that it is not worth using a precise 24-bit ADC for sound recording if we don't have an *ultra low jitter* clock. One should consider taking this phenomenon into account before choosing an ADC.

D/A Converter



D/A Converter of weighted R (1/4)

From a single constant reference voltage (V_{ref}) are taken n weighted currents through n switches S_0, S_1, … S_{n-1}



On each switch S_i it is placed a resistence $r_i=2^{(n-1)-i}R$

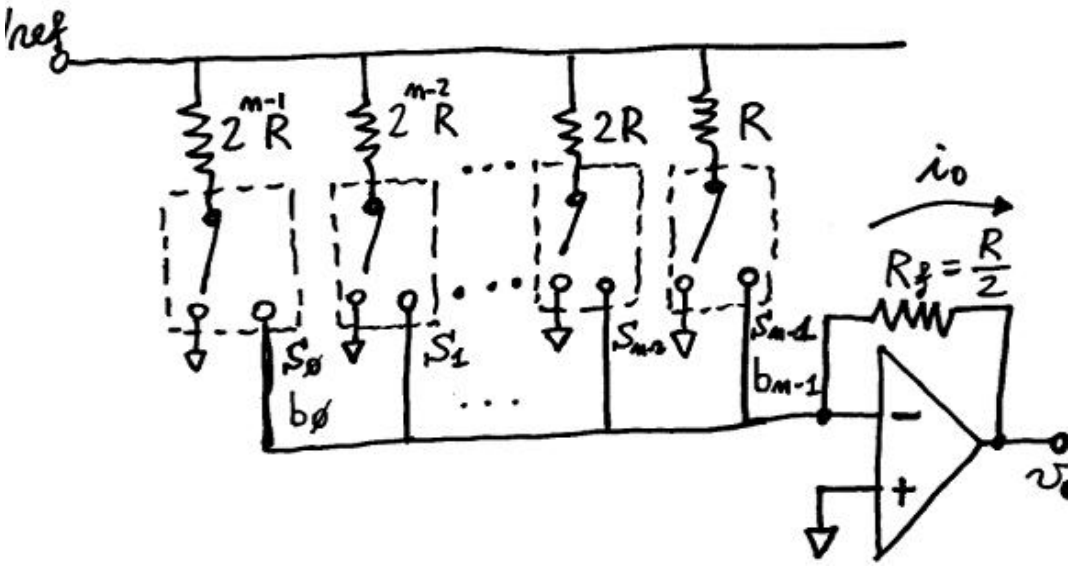
D/A Converter of weighted R (2/4)

The switches s_i are controlled by binary digits b_i of the number to be converted in voltage, with weights:

b_0 = LSB Least Significant Bit

b_{n-1} = MSB Most Significant Bit

The operational amplifier acts as a weighted adder of the currents which pass through the switches and converts the resulting current i_0, through the feedback resistor R_f, into an output voltage v_0

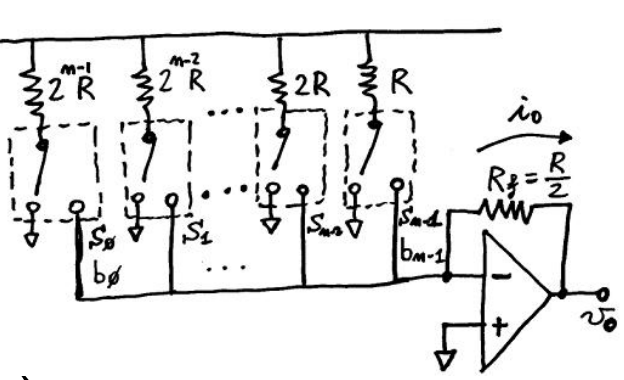


D/A Converter of weighted R (3/4)

The weighted currents are

$$i_i = \frac{V_{\text{ref}}}{2^{(n-1)-i}R} = 2^i \frac{V_{\text{ref}}}{2^{(n-1)}R} = 2^i I_{\text{mi}}$$

(n bit)



with $i = 0, 1, \ldots, n\text{-}1$ (like the digits)

The total current through the closed switch (S_i is closed — dx position — when b_i=1) è

$$i_0 = \frac{V_{\text{ref}}}{2^{(n-1)}R}\left(b_0 + 2b_1 + \ldots + 2^{n-2}b_{n-2} + 2^{n-1}b_{n-1}\right)$$

D/A Converter of weighted R (4/4)

The output voltage is:

$$v_0 = -R_f I_0 = \left(b_0 + 2b_1 + \ldots + 2^{n-1} b_{n-1}\right)\frac{V_{\text{ref}}}{2^n}$$

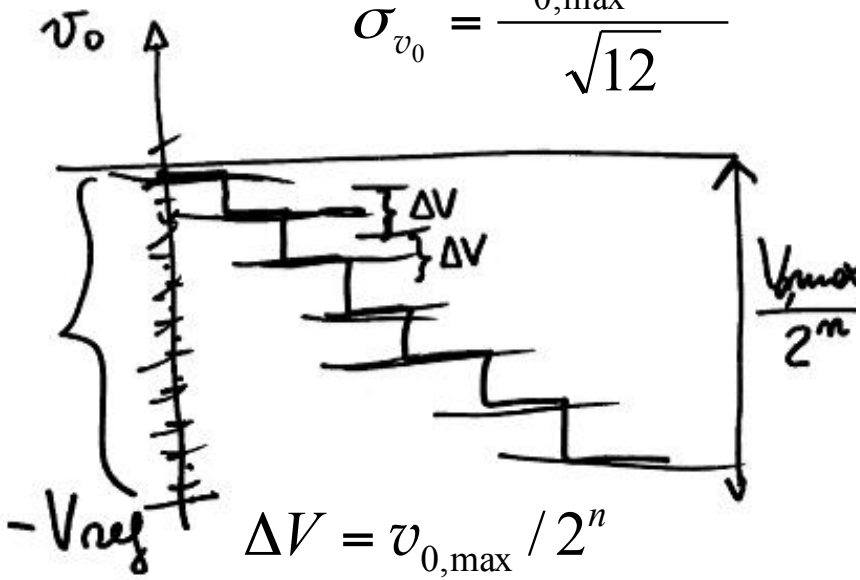
$$v_0 = \left(b_0 + 2b_1 + \ldots + 2^{n-1} b_{n-1}\right)\Delta V = k\,\Delta V$$

with k integer number, within 0 e 2^{n-1}

The accuracy of DAC is releted with V_{ref}, single resistence r_i and the quality of the switches

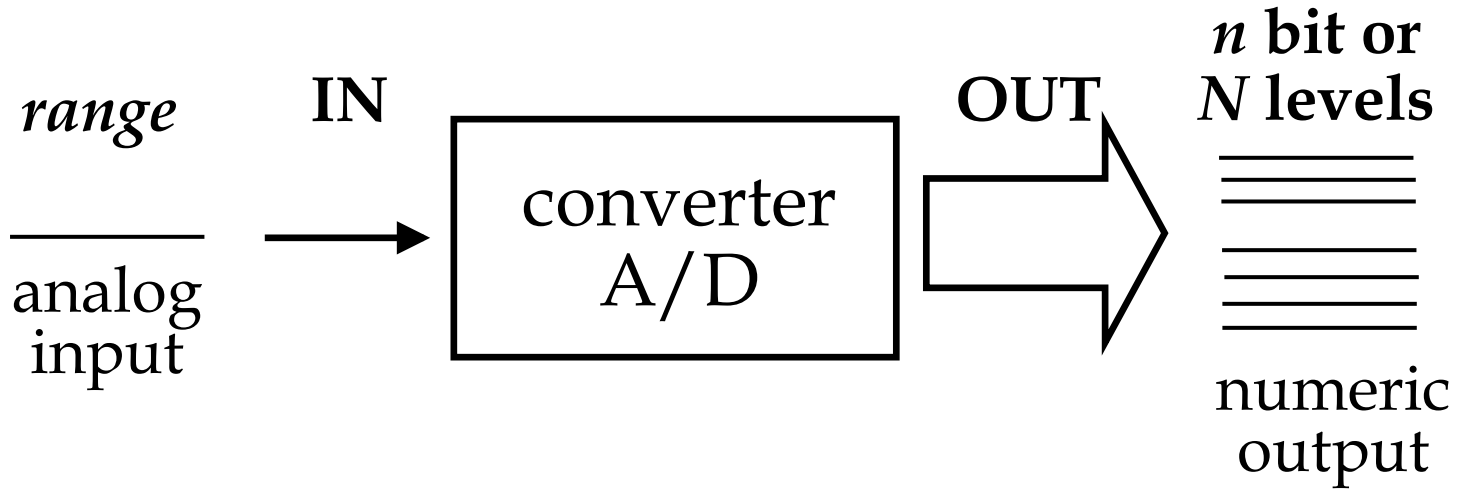
The values of analog output voltage V_0, coming from digital samples at n bit, have a **resolution of $\Delta V = v_{0,\max}/2^n$**

$$\sigma_{v_0} = \frac{v_{0,\max}/2^n}{\sqrt{12}}$$



$$\Delta V = v_{0,\max}/2^n$$

Converter A/D



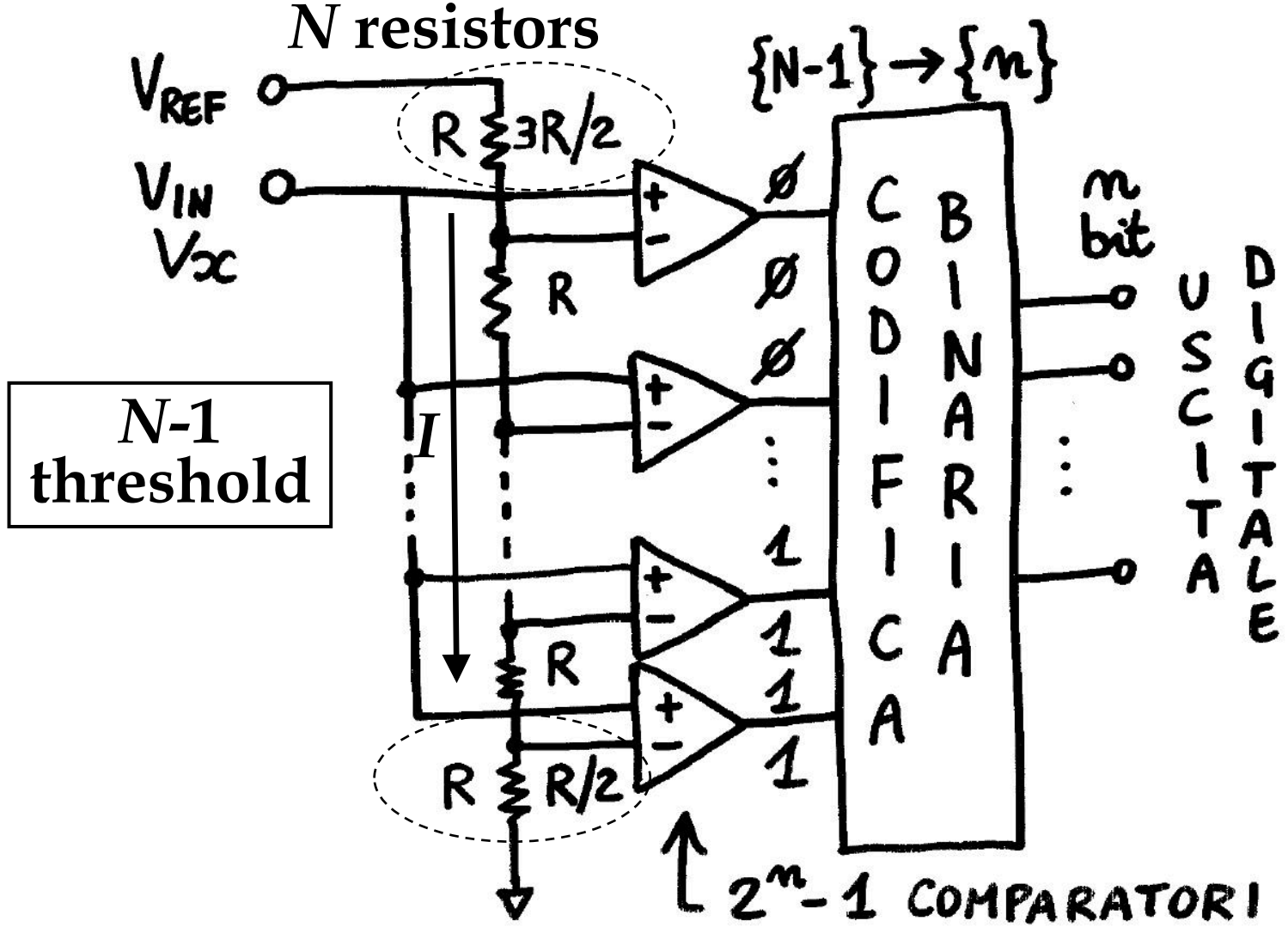
Voltmeter – Flash converter(1/4)

It is the fastest A/D converter with $T_{\text{meas}} \approx 1\ T_{\text{s}}$ and conversion frequency up to 40 GSa/s

The circuit complexity (and the expense) increases exponentially with the number of bits (as 2^n) and then it works at low resolution:

$$n \sim 8 \text{ bit}$$

Voltmeter – Flash converter (2/4)



Voltmeter – Flash converter(3/4)

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N resistors same values

$$I = \frac{V_{\text{ref}}}{NR} \qquad V_i = i\underbrace{(RI)}_{\Delta V} = i\underbrace{\frac{V_{\text{ref}}}{N}}_{\Delta V} \qquad i = 1, \ldots N - 1$$

N-1 threshold

First and last resistors are different

$$I = \frac{V_{\text{ref}}}{2R + (N-2)R} = \frac{V_{\text{ref}}}{NR}$$

$$V_i = \left[\frac{R}{2} + (i-1)R\right] I = \left(i - \frac{1}{2}\right)\frac{V_{\text{ref}}}{N} \qquad N - 1 \text{ threshold}$$

With the network of resistors 3/2 R and R / 2 the threshold for the 1st level is halved in amplitude which is useful to have no offset in the characteristic of conversion and to convert bipolar signals.

1st and Nth levels are different

Exercise (Flash converter)

Broadband digital oscilloscope

Range $D = \pm 10$ V $\quad n = 8$ bit $\quad f_{\text{sample}} = 1$ GSa/s

$\Delta V = ?$ $\qquad \Delta V = \dfrac{D}{2^n} = \dfrac{20\text{ V}}{256} \cong 80\text{ mV}$

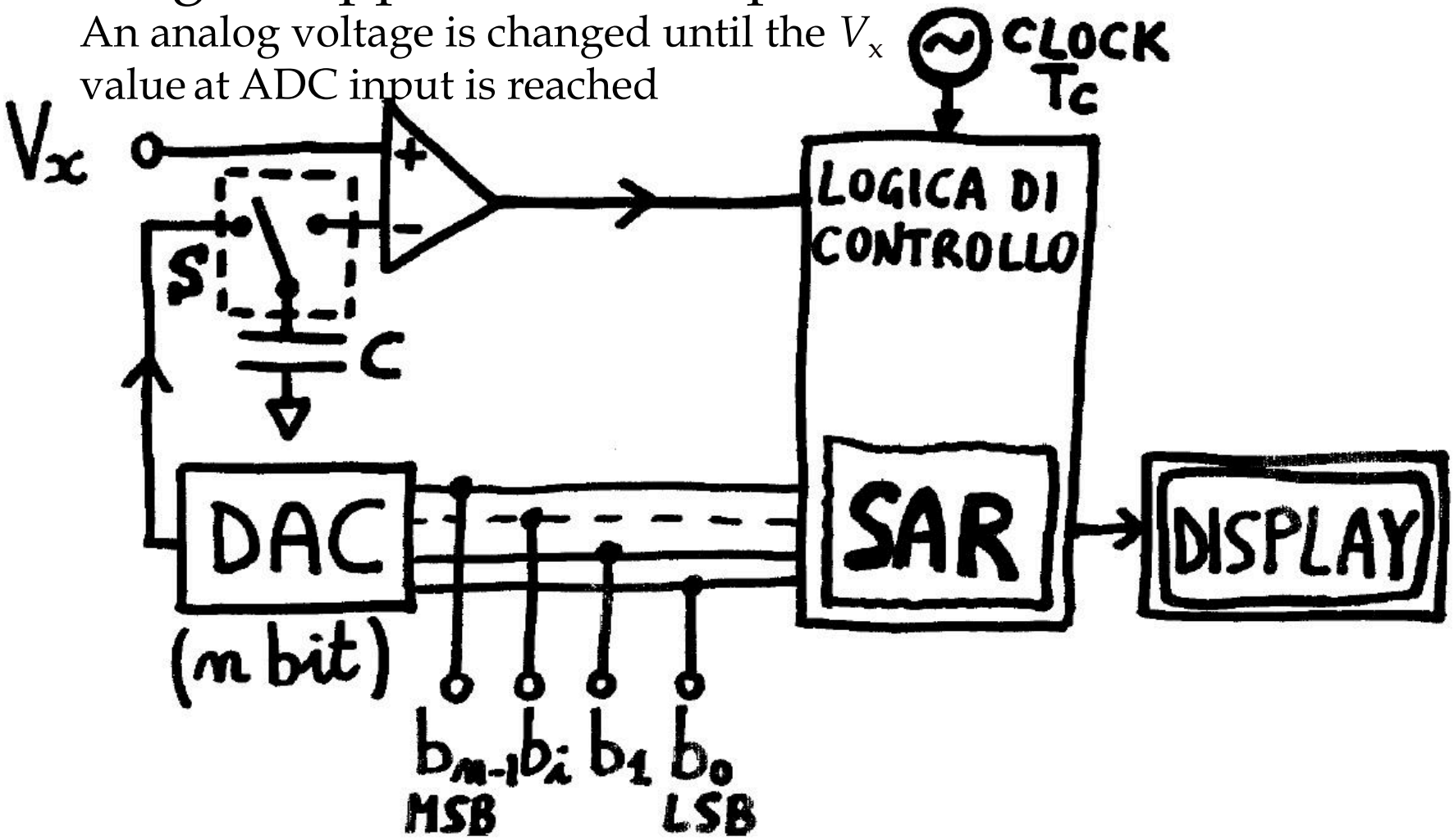
$\sigma_V = u(V) = ?$ $\qquad u(V) = \dfrac{\Delta V}{\sqrt{12}} \cong 23\text{ mV}$

$f_{x,\max} = ?$ $\qquad f_{\text{x, max}} = f_{Sample} / 2 = 500\text{ MHz}$

Successive approximations Voltmeter (1/6)

Digital approach to the potentiometric method

An analog voltage is changed until the V_x value at ADC input is reached



Successive approximations Voltmeter (2/6)

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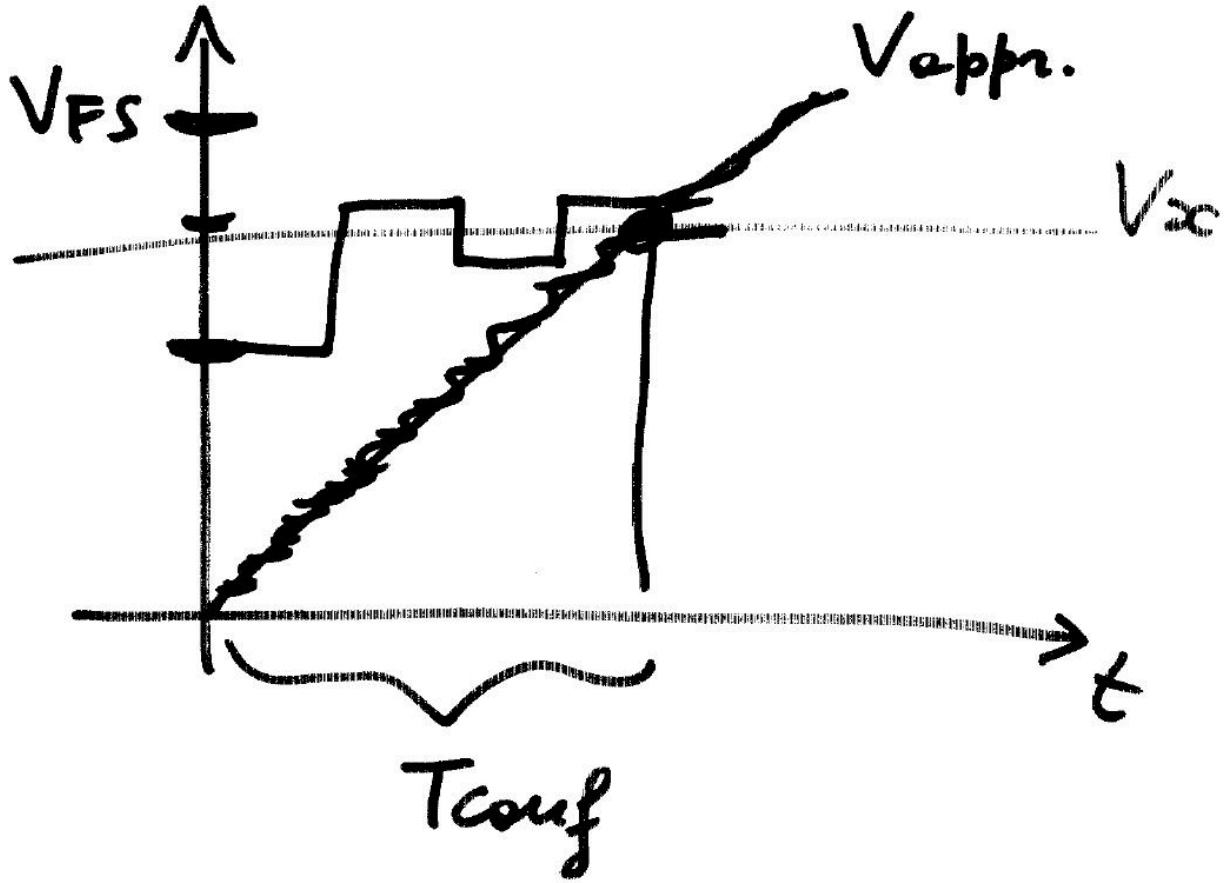
- *n* bit D/A converter
  Comparator and control logic
  Clock (timing of the system)

- With the **BISECTION method** are "tested" all the bit (value=1) starting from the most significant (MSB) up to the less significant (LSB)
  For each comparison with V_x it is decided wheter to keep the bit "1" or reset it to "0"

$$\text{DAC output: } V_{D/A} = \underbrace{\frac{V_{FS}}{2^n}}_{\Delta V}\left[b_{n-1}2^{n-1} + \ldots + b_1 2 + b_0\right]$$

Successive approximations Voltmeter (3/6)



With only ***n*** **comparison** it is achieved a **resolution $\delta = 1/N = 1/2^n$**

Successive approximations Voltmeter (4/6)

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- The less significant value (b_0) has a WEIGHT

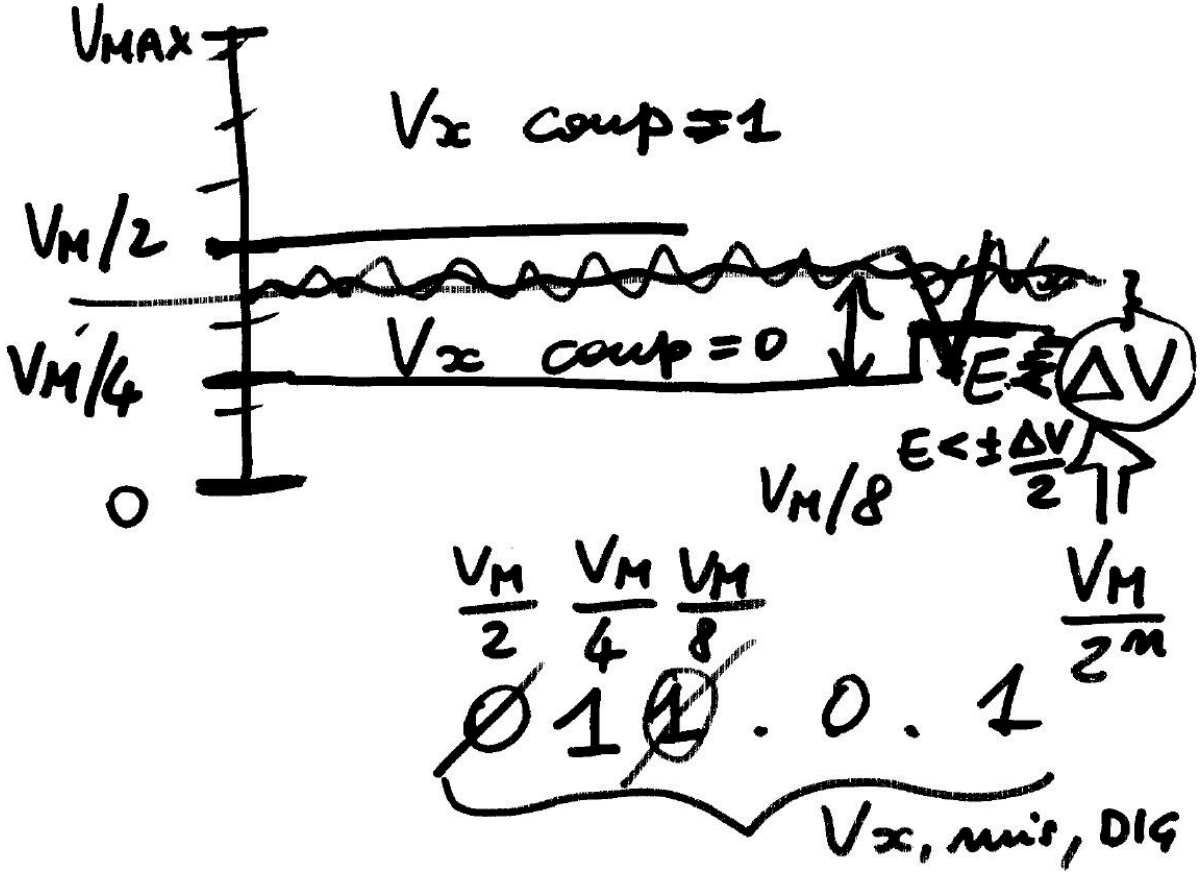
  $$\Delta V = V_{FS} / 2^n \quad \leftarrow \quad N = 2^n$$

  The most significant one (b_{n-1}) is equal to $V_{FS} / 2$

- **"Only" $n = \log_2 N$ comparisons** ciascuno are made of lenght $T_{comp.} = mT_c$ with m included between 2 and 5

- The acquisition time is set regardless of V_x value and is equal to $\boldsymbol{T_{acq.} = n\, T_{comp.}}$
  The sampling frequency is $f_{acq.} = 1/T_{acq.}$

Successive approximations Voltmeter (5/6)



The differential noise can lead "instantaneously" to wrong decisions on the individual comparison and so to an acquisition

Successive approximations Voltmeter (6/6)

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- **Real resolution** (from 3 to 5 "equivalenti" digit) is releted with the noise present at the input stages of the comparator (is not always $V_{FS} / 2^n$...)

- **Accuracy**: it is releted with the internal reference, the quality of DAC and the comparator noise

- STATE OF ART:

n [bit]	12	16	18 (5½ digit)
T_{mis} [μs]	2	5	20 (50 kSa/s)

Performaces of successive approximations voltmeter

These voltmeters are also quite fast while maintaining excellent resolution (*e.g.* $T_{\text{mis}} = 5\ \mu$ s, so $f_{\text{sample}} = 200$ kSa/s with $n = 16$ bit)

Low pass filter input to limit the "wrong decisions" due to the noise input so it also reduces the speed of conversion

Exercise (SAR voltmeter)

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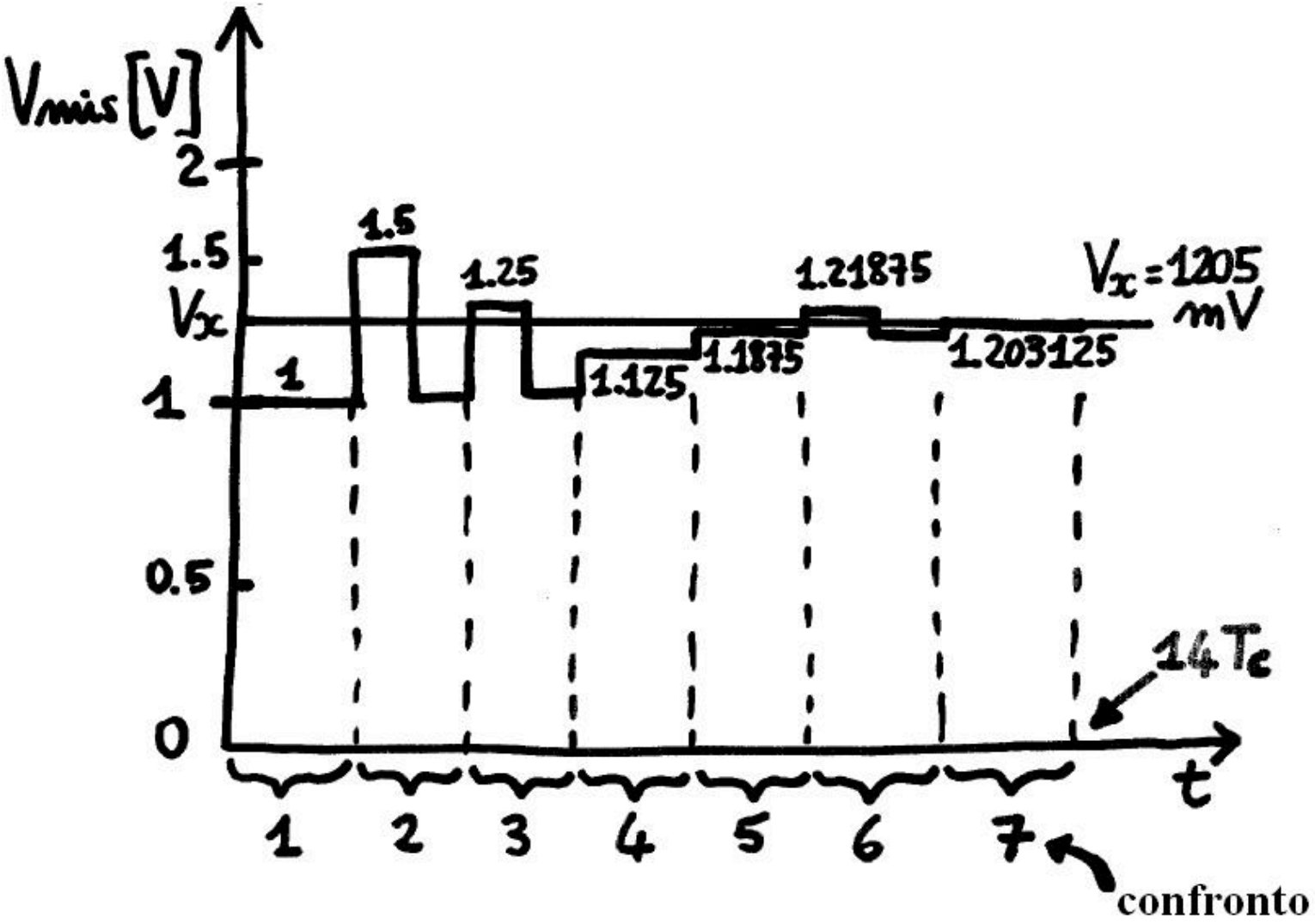
Range 0 - 2 V $\quad n = 7$ bit

$f_{clock} = 1$ MHz $\quad T_{comp.} = 2\,T_c$

Indicate the total time of measurement, the measured value V_{meas} displayed and its error rate compared to a voltage to be acquired of $V_x = 1205$ mV

Solution (1/2)


Vmis [V]
2
1.5
1
0.5
0
Vx
1
1.5
1.25
1.125
1.1875
1.21875
1.203125
Vx = 1205 mV
14 Tc
t
1
2
3
4
5
6
7
confronto

Solution (2/2)

$$T_c = 1/f_c = 1\,\mu\text{s}$$

$$T_{confr} = 2T_c = 2\,\mu\text{s}$$

$$T_{acq} = T_{mis} = nT_{confr} = 14\,\mu\text{s}\ (\approx 70\ \text{kSa/s})$$

$$V_{mis} = 1203.125\ \text{mV}$$

$$\text{ERR}\% = \frac{|V_x - V_{mis}|}{V_x} = 0.1556\,\%$$

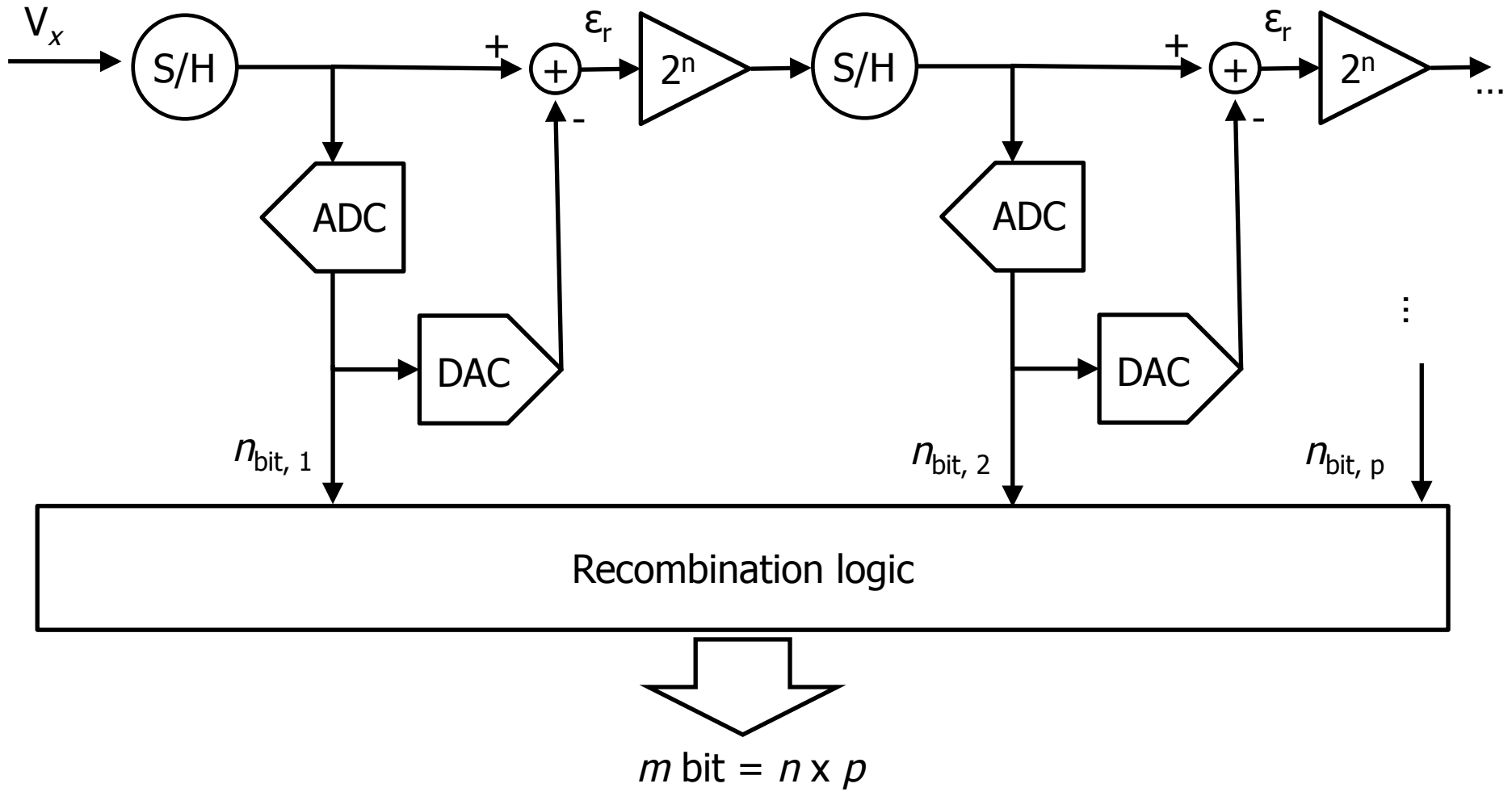
With only 7 bit it is achieved a resolution of:

$$\Delta V = \frac{V_{max}}{2^n} = \frac{2V}{128} \cong 15.6\ \text{m}V$$

In a practical case, for example with 12 bits instead of 7, it would gain a factor of 32 ($2^5=2^{12-7}$) and the resolution would become $\Delta V_{12bit} \cong 500\ \mu\text{V}$

ADC pipeline (1/4)

Architecture:



ADC pipeline (2/4)

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The A/D converter pipeline uses the principle of the assembly line: in practice, the V_x input signal is converted, in successive steps, by p cascaded stages. While the first stage processes the current sample of the input signal, the second stage further processes the sample, already processed by the first stage in the clock period preceding, and so on, right down to the last stage.

Each of the stages produces an $n_{bit,\,p}$ of m_{bit}, that make up the digital output word. The pipeline converter, therefore, apart from an initial latency of p clock periods (pTCK), provides in output a new digital word for each clock period (TCK), as the flash converter. Each of the p stages of the A/D converter converts the pipeline in its digital input signal, with a given resolution ($n_{bit,\,p}$), and supplies at the output the corresponding digital word in $n_{bit,\,p}$ bits, as well as a residue, which must be then converted by the next stage

ADC pipeline (3/4)

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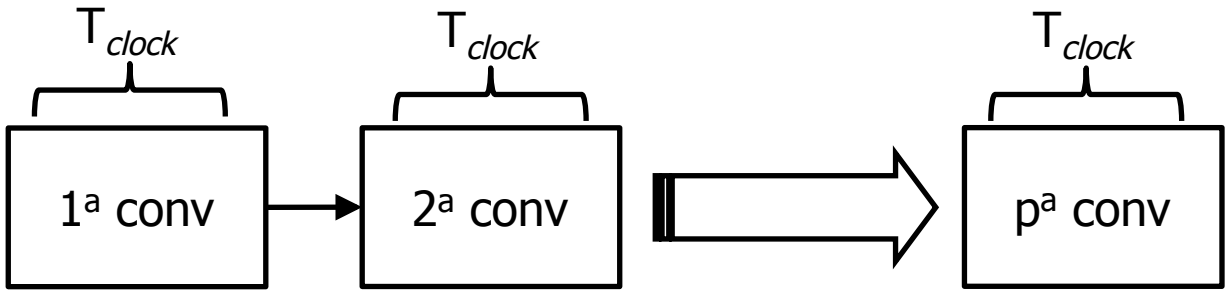
The residue obtained by multiplying for 2^n the difference between the input signal of the stadium and the output $n_{bit,\ p}$ signal, converted to analog by a D/A converter. The residue is, therefore, substantially, the quantization error introduced by each stage in the A/D conversion to $n_{bit,\ p}$ bit. The bits obtained in output from the different stages are then realigned via appropriate registers, so as to form the digital output word *m*, corresponding to each sample of the input signal. The resolution of a pipelined converter is limited by the accuracy with which they manage to achieve ε_r factors, required to generate the residue, as well as by the precision of the A/D and D/A converters, built-in in the individual stages typically constituted by flash A/D converters.

The most important stage for the accuracy of the measurement is the first from which is obtained the most significant bit (MSB). Usually you use a converter with one bit more than the subsequent.

Performance: The maximum resolution achievable is around 24 bits by a minimum of 8 bits with frequencies ranging from 1 MSa / s to 200 Msa / s.

ADC pipeline (4/4)

Latency time: is the time required for the first converted sample to be available at the output of the converter. In the case of A/D pipeline, latency time will be equal to the time required for the first sample has passed through all the stages, so it will be equal to the clock period (TCk) multiplied the number of stages.
It is to be noted that the conversion time differs from the latency time, since already from the second sample I must wait one clock interval (TCk) to have the data available on the output.



Latency Time= T_{clock} x p

Conversion Time= T_{clock}